into hole currents, which then flow through the PMOS1 180 channel and into the cathode contact. An N-channel depletion mode MOSFET (NMOS) 188 is also integrated at the surface of the SECT which acts as the turn-on MOSFET. A second PMOSFET (PMOS2) 190 is formed between the turn-on NMOS 188 and the PMOS 1 180 with the upper P base acting as its source. The NMOS 188 and the PMOS2 190 share the same gate, and the gate is directly tied to the cathode contact 192, hence, the SECT is a three-terminal device.

B4 cont'd.

In the claims:

Please substitute the following claims 1, 19 - 24, 33, 34 and 37 for the like-numbered claims as previously filed. A marked up copy of these claims showing the current changes is attached as an appendix to this amendment.

1. (Amended) An emitter controlled thyristor device having a cathode terminal and an anode terminal, comprising:

B5

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

fig. 5A&B C1

a first metal oxide semiconductor transistor (MOS) connected in series with said thyristor between said cathode terminal said thyristor emitter, said first MOS transistor integrated in at least one of the semiconductor regions of said thyristor; [and]

a second MOS transistor integrated in at least one of said semiconductor regions connected between said cathode terminal and said thyristor gate, a gate terminal of said second MOS transistor connected to said cathode terminal; and

P, 5, 6 19

means for injecting electrons into said thyristor for triggering said thyristor into [said latching state];

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode terminal turning said emitter controlled thyristor device to an on state, and a zero to second voltage turns applied to said gate of said first MOS transistor turns said emitter controlled thyristor device to an off state.

19. (Amended) An gate turn-off (GTO) thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal plate;

a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said GTO thyristor device package;

a first metal oxide semiconductor (MOS) transistor positioned on said second metal plate adjacent said thyristor, said first MOS transistor having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for [said ETO device package]; and

a second MOS transistor positioned on said second metal plate adjacent said thyristor, said second MOS transistor having a first terminal connected to a gate of said thyristor, said second MOS transistor further having a second terminal and a gate terminal connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns [said emitter controlled thyristor device] to an off state.

20. (Amended) A gate turn-off (GTO) thyristor device package as recited in claim 19, further comprising a clamp means for holding said first, second and third metal [layers] plates together.

21. (Amended) A gate turn-off (GTO) thyristor device package as recited in claim 19, wherein said first, second and third metal plates comprise copper plates.

22. (Amended) A gate turn-off (GTO) thyristor device package as recited in claim 39, wherein [said first and second switches are first and second MOS transistors], respectively, and said first MOS transistor and said second MOS transistor are complementary.

23. (Amended) A gate turn-off thyristor (GTO) device package comprising:

a gate turn-off (GTO) thyristor comprising a thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a plurality of MOS transistors connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said MOS transistors connected to said thyristor emitter and a second terminal of said MOS transistors connected to a cathode terminal of said GTO device package; and

a plurality of switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said [MOS] switching devices connected to said thyristor gate and a second terminal of said switching devices connected to said cathode terminal of said GTO device package,

wherein a first voltage applied to a gate terminal of said MOS transistors turns said GTO thyristor to an on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate of said MOS transistors

turns said GTO thyristor to an off state.

24. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23, further comprising:

a first metal plate forming said cathode terminal;

a second metal plate separated from said first metal plate by an insulation layer, wherein said GTO thyristor and said MOS transistors and [said switching devices] are positioned on said second metal plate, said first and second metal plates acting as a heat sink.

25. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 further comprising a third metal plate forming [and] anode terminal of said GTO thyristor device package.

26. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein [said switching devices] comprise a MOSFET transistor having a gate connected to said cathode terminal.

27. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein [said switching devices] comprise a diode.

28. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein [said switching devices] comprise a diode connected in parallel with a capacitor.

29. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein [said switching devices] comprise a Zener diode connected in parallel with a capacitor.

30. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein [said switching

devices] comprise a transistor connected in parallel with a capacitor.

31. (Amended) A gate turn-off thyristor (GTO) device package as recited in claim 26 further comprising;

a first feedback path connecting said gate terminal of [each of said MOS transistors] to said thyristor emitter; and

a second feedback path connecting said gate terminal of [each of said MOS transistors] to [said thyristor gate terminal] through a diode.

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33. (Amended) An emitter turn-off thyristor device including

a thyristor device having an anode terminal, a cathode terminal and a gate terminal,

a first semiconductor switch in series with said cathode terminal of said thyristor device by a first terminal of said first semiconductor switch,

[as] a second semiconductor switch in series with said gate terminal of said thyristor device by a first terminal of said second semiconductor switch; second terminals of said first and second semiconductor switches being connected together, and

means for shorting said emitter of said thyristor element to a terminal of said first switch or for injecting electrons into said thyristor for triggering said thyristor into [said latching state];

wherein [said first and second semiconductor switches are arranged such that a signal of a first type applied to said first and second electronic switches turn said emitter turn-off thyristor to an on-state and a signal of a second type applied [to control electrodes of] to said first and second electronic switches turn said emitter turn-off thyristor to an off-state].

B7 cont. discrete switch in claim 33

34. (Amended) [An emitter turn-off thyristor] as recited in claim 33, wherein [said thyristor device] and at least one of said first and second semiconductor switches [are formed monolithically].

Sub D1 / B8

37. (Amended) [An emitter turn-off thyristor] as recited in claim 33, wherein at least one of said first and second semiconductor switches is an MOS device.

Please add the following new claims 39 - 41, as follows:

39. A GTO device package as recited in claim 19, wherein one of [said first and second switches] is a MOS transistor.

fig. 18 B9

40. A GTO device package as recited in claim 19, wherein one of [said first (112 1st)] and second switches] is [a diode (112 2nd)].

fig. 18

41. A GTO device package as recited in claim 19, wherein one of [said first (112 1st)] and second switches is [a zener diode (112 2nd)].

42. [A GTO device package as recited in claim 33], wherein one of said first and second switches is a MOS transistor.

fig. 18 sub C1

43. [A GTO device package as recited in claim 33], wherein one of [said first (112 1st)] and second switches [is a diode].

fig. 18

44. [A GTO device package as recited in claim 33], wherein one of [said first (112 1st)] and second switches [is a zener diode].